

REMARKS

This amendment is responsive to the Official Action dated June 26, 2003.

Claims 1-27 and 29-34 were pending in the application. Claims 1-3, 5-10, 13, 14, 19, 21, 23, 26, 27 and 29 were rejected. Claims 4, 11, 12, 15-18, 20, 22, 24 and 25 were objected to. Claims 30-34 were allowed.

By way of this amendment, the Applicant has amended claims 1 and 19.

Accordingly, claimed 1-27 and 29-34 are currently pending. Favorable reconsideration of all claims is respectfully solicited in view of the Remarks below.

I. Rejections under 35 USC § 112:

Claims 27-29 were rejected under 35 USC §112, first paragraph as lacking support within the specification. The Applicant has amended Claims 27 and 29 to revise the language to read a "highly electrically resistive" region rather than an electrically isolated region.

With regard to claims 27 and 29, the appropriate support for the claim language as amended is found in Fig. 20 as viewed in connection with the disclosure on Page 20, lines 11-14. Clearly the disclosure states that n-type layer 510 can be implanted to increase its resistivity without rendering it fully insulative. The specification discloses the conductive layer 510 may be implanted to form a resistor, elements 560(a) and 560(b) form the resistor contacts, and the resistor path is 560(a) through implanted layer 510 to 560(b). 560(a) and 580(c) form a capacitor pair.

Withdrawal of the rejection and reconsideration of the rejection is respectfully solicited.

II. Rejections under 35 USC §102:

Claims 1-3, 5, 7, 10, 13, 19, 21, 23 and 26 were rejected under 35 USC §102 as being unpatentable over the US Patent to Flynn. The Examiner has asserted that Figs. 1, 2 and 3Q illustrate a photodetector 20, 30 and capacitor 22, 35A, 42 coupled between the photodetector bias terminal and ground.

Referring to Fig. 1 of the present invention, there is disclosed a photodiode 10 having anode 14 and cathode 16, and a transimpedance amplifier (TIA) 20 having an input terminal 18 connected to anode 14, and a ground terminal. A bias terminal 12 is connected to the cathode 16. In the present invention, in contrast to the disclosure in Flynn, a capacitor 22 is shunted between the cathode 16 and the ground 24. In this arrangement, continuous bias is

applied to the cathode 16 of the photodiode. The capacitor 22 capacitively couples the bias terminal (power supply voltage Vcc) to the AC ground of the TIA at the point where the un-amplified current signal generated by the photodetector is passed to the TIA. The capacitor is thus a path to pass AC signal from the bias terminal to ground. The on-chip capacitor eliminates the inductance of external circuit traces between the power supply and an external capacitor. Claims 1 and 19 as amended clearly include the limitation of a continuously applied bias to the bias terminal 12.

Referring to Flynn (Fig. 1) there is disclosed capacitor connected in series with the anode and cathode of the photodiode. In this arrangement the capacitor is intended to store a charge from the photodiode. It essentially acts as a memory element for the photodiode which is periodically read in a scanning operation. Flynn shows a ground at 64 and a voltage supply Vcc at 60. The ground 64 is coupled to the PD/C series circuit between one terminal of the capacitor and the anode of the PD. As far as understood by the Applicant, the cathode of PD 20 is not biased as currently claimed. The cathode terminal of the PD is connected to a logic gate at 38 which is normally open until it is desired to read (dump) the charge from the capacitor. At polling, the capacitor charge is shunted to a sensing amplifier.

In summary, the capacitor in Flynn is not believed to be coupled between the photodetector AC ground and the photodetector bias terminal to provide a continuous bias to the photodetector as clearly indicated in the claims as presently amended. The capacitor in Flynn acts as a memory element to store information about the level being sensed by the photodetector, while the capacitor in the present invention serves to provide a continuous path to AC ground. The underlying functionality is entirely different and thus the underlying structural connections are also different.

Favorable reconsideration of the rejected claims is respectfully solicited.

III. Rejections under 35 USC §103:

Claims 6-10 and 14 were rejected under 35 USC §103 as being unpatentable over Flynn. The Examiner has asserted that the claimed materials are well known for use as a dielectric in the art.

In light of the above-noted Remarks with respect to Flynn and the underlying claims, the present rejection is not longer believed to be applicable. Favorable reconsideration is respectfully solicited.

IV. Allowable claims:

Claims 30-34 were determined to be allowable over the prior art of record.

Applicant further acknowledges the allowability of claims 4, 11, 12, 15-18, 20, 22, 24 and 25 if rewritten to include all of the subject matter of the intervening claims. Applicant shall withhold rewriting of these allowable claims until reconsideration of the presently amended base claims and the above arguments with respect to Flynn has been determined.

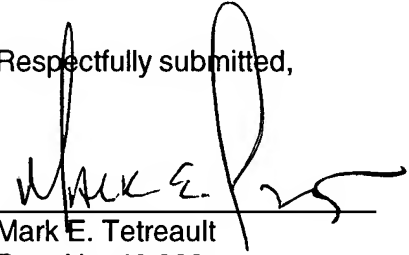
V. CONCLUSION

Accordingly, claims 1-27 and 29-34 are believed to be in condition for allowance and the application ready for issue.

Corresponding action is respectfully solicited.

PTO is authorized to charge any additional fees incurred as a result of the filing hereof or credit any overpayment to our account #02-0900.

Respectfully submitted,


Mark E. Tetreault
Reg. No. 48,289

BARLOW, JOSEPHS & HOLMES, Ltd.
101 Dyer Street, 5th Floor
Providence, RI 02903
401-273-4446 (tel)
401-273-4447 (fax)